**module rc (clk, init, count);**

**input clk, init;**

**output [7:0] count;**

**reg [7:0] count;**

**always @(init or posedge clk)**

**begin**

**if (init)**

**count = 8'b10000000;**

**else begin**

**count <= count << 1;**

**count[0] <= count[7];**

**end**

**end**

**endmodule**

**module test\_rc;**

**reg clock;**

**reg reset;**

**wire[7:0] out;**

**rc r1 (.clk(clock), .init(reset), .count(out));**

**always**

**#5 clock = ~clock; //toggle clk every 5 time units**

**initial**

**begin**

**clock = 1'b0; //set clk to 0**

**reset = 1'b1;**

**#12**

**reset = 1'b0;**

**#200 $finish; //terminate the simulation**

**end**

**initial**

**$monitor($time, ": Output = %b", out);**

**endmodule**